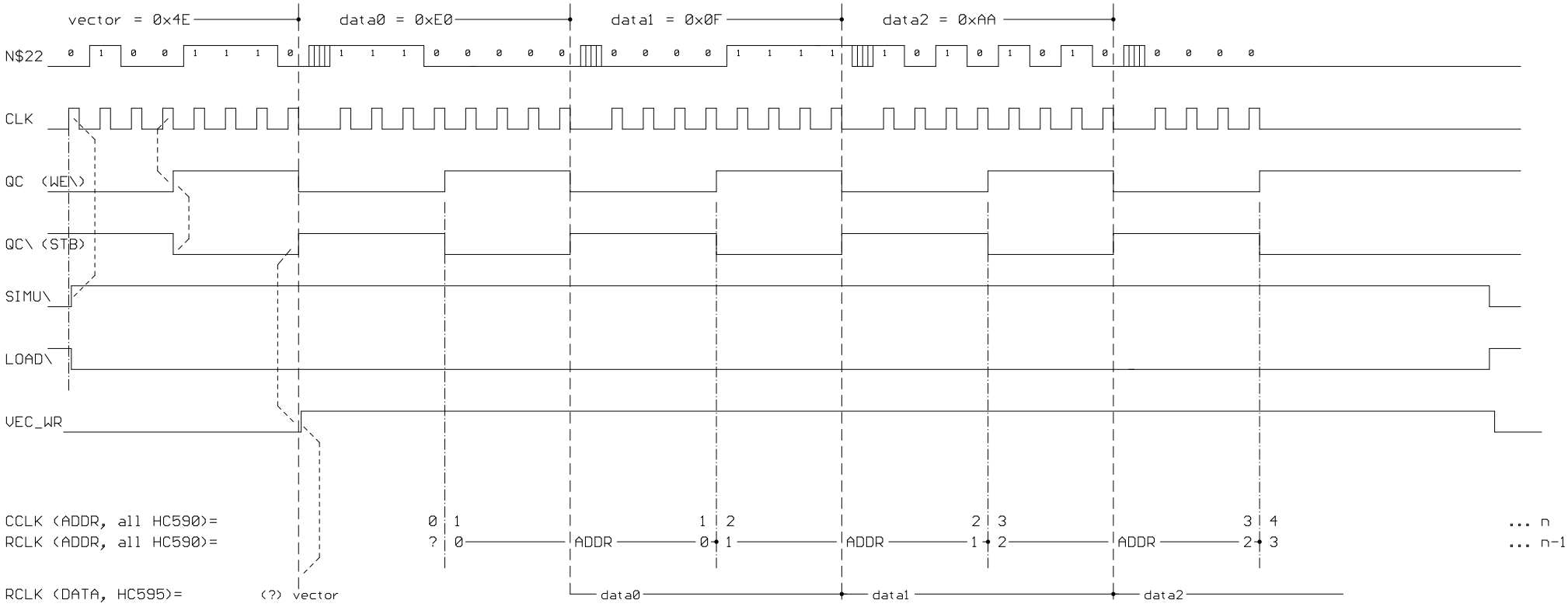
timing diagram ESIMU2



"dual edge loading" (QC pulse)

-on rising edge (QC\): load shifted data into output register (RCLK), data valid

-on rising edge (QC): end of writing data into selected RAM
inc address value in counters and load previous addr count into output register (RCLK)

- remark: counter cclk and rclk differ for one clk period (rclk = cclk + 1)

- The VLOAD pulse loads the eprom type vector.
  The address latches are undefined during VLOAD pulse, but this doesn't matter.

- to close the last write access, there is a need of four clk pulses

- very important: during low period of WE\ address value must be stable.
  data writing into RAM is level and NOT edge triggered !!

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